P27110.A05

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	: Paul A. HYDE	Group Art Unit: 2857
Appln. No.	: 10/711,224	Examiner: Mohamed Charioui
Filed	: September 2, 2004	Confirmation No.: 5223
For	: SELF HEATING MONITOR FOR SIGE AND SOI CMOS DEVICES	

DECLARATION UNDER 37 C.F.R. 1.131

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

We, Paul A. Hyde and Edward J. Nowak do hereby declare:

1. We are the inventors of the subject matter disclosed and recited in at least independent claims 1, 25, 34 and 39 of the above-identified application.

2. We completed the invention of claims 1, 25, 34 and 39 (and those claims dependent thereon) in the United States before July 27, 2004, as evidenced below.

CONCEPTION

3. Before July 27, 2004, we conceived of the following matter recited in claims 1, 25, 34 and 39:

1. A method of measuring performance of a device, comprising:

thermally coupling a first heating device to a first sensing device;

generating heat at the first heating device;

measuring a change in at least one electrical characteristic of the first sensing device caused by the heat generated at the first heating device; and

calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic.

25. A method of measuring performance of a device, comprising:

thermally coupling a heating transistor to a measurement transistor at one or more predetermined distance;

calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature;

generating heat at the heating transistor;

incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor; and

calculating a temperature of the heating transistor using the measured change in the at least one electrical characteristic.

34. An apparatus for measuring semiconductor device temperature, comprising:

a silicon island;

at least one pair of transistors, each pair of the at least one pair of transistors comprises a transistor configured to generate heat and a transistor configured to sense temperature;

the transistor configured to generate heat and the transistor configured to sense temperature being arranged on the silicon island; and

a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature,

wherein each transistor of each pair of transistors is arranged a prescribed distance from its corresponding transistor.

39. An apparatus for measuring semiconductor device temperature, comprising:

at least one silicon island;

at least one heating field effect transistor configurable to generate heat arranged within the silicon island;

at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature; and

means to calculate a temperature of the each heating field effect transistor using a measured change in at least one electrical characteristic of the each sensing field effect transistor caused by the heat generated at the each heating field effect transistor.

4. Evidence of such conception as disclosed and recited in claims 1, 25, 34 and 39 of the application, is shown in IBM Invention Disclosure labeled "BUR8-____-0245" and accompanying figures, which textually and pictorially show the features of independent claims 1, 25, 34 and 39 (and the dependent claims). See Exhibit A attached hereto. The documents attached hereto are photocopies of and are substantially identical to the original, except that certain pertinent dates have been removed therefrom.

5. Relevant dates removed from the IBM Invention Disclosure labeled "BUR8-____-0245" are before July 27, 2004.

6. The benefits and features of the recited invention are shown and described in the Invention Disclosure.

7. These features and others are exemplified in the figures accompanying the Invention Disclosure.

DUE DILIGENCE

8. Inventor Edward J. Nowak communicated with IBM in house patent agent Anthony J. Canale and outside patent counsel, Andrew M. Calderon and Randall Cherry, in preparing a patent application based on the Invention Disclosure.

9. We worked diligently on the preparation of the patent application by first submitting the invention disclosure statement to in-house IBM counsel.

10. After the invention disclosure was mailed to outside counsel, Andrew M. Calderon, we worked diligently on the preparation of the patent application with outside patent counsel Andrew M. Calderon and Randall Cherry until a final draft patent application was completed to our satisfaction. Communications took place on at least March 20, 2004, and thereafter, prior to July 27, 2004.

11. A final draft of the patent application was forwarded to IBM counsel on August 25, 2004 for execution of the formal documents by all of the inventors. We signed the documents for filing in the U.S. Patent and Trademark Office, which was effectuated on September 2, 2004.

12. We declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Paul A. Hyde — 11/15/2007

Paul A. Hyde — Date

Edward J. Nowak — 15 Nov 2007

Edward J. Nowak — Date

EXHIBIT A

{P27110 00294199.DOC}

Main Idea for Disclosure BUR8[redacted]0245
Prepared for and/or by an IBM Attorney - IBM Confidential
Archived O[redacted]01:22:42 AM

Title of disclosure (in English)
Self-Heating Monitor for SiGe and SOI CMOS.

Main Idea of disclosure

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.
Accurate measurement of self-heating on SOI and SiGe-based MOSFETs is important because the measured DC currents are typically depressed significantly due to self-heating while in CMOS circuits transients are too rapid for significant self-heating to occur. Thus simulation (compact) models must be adjusted to correctly account for self-heating in order to correctly predict circuit performance. In SOI technologies this effect ranges from 3% to 12% while in SGOI (SiGe on SOI) these effects are expected to exceed 30%. This invention describes structures and a technique which with only low-cost, simple, manufacturable DC measurements allows an accurate

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.
Previous work relied on transient measurement to avoid self-heating. This requires good body contacts to avoid interference from dynamic body effects and has become ineffective because the body contact time constants have become too long. Another technique was to use body-to-source junction characteristics to monitor temperature rise, but this too has become impractical due to the combination of very poor junctions and high resistance to the body in the contacted structures.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.
The Structures in this invention consist of a silicon island with two FETs imbedded within. One FET is used to heat the island and the second FET is used to measure the temperature. This is done by calibrating some characteristic of the 'measurement FET', such as subthreshold swing, vs ambient temperature while the 'heating FET' has no power applied. Then one can monitor this characteristic (e.g. swing) vs power dissipated in the 'heating' FET and infer the temperature rise above the ambient at the 'measurement FET'. Since the temperature of the silicon island will be very non-uniform, one must use several such structures with varying separation between the two FETs and then extrapolate to the temperature rise at the heating device.

Attached below are some details:

10S Alta self heating test results

Created By: Paul Hyde on[redacted]at 02:40 PM
Category: Self Heating

These measurements are 10S self heating. The structures were designed by Ed Nowak and can be found on the Alta testsite. Subthreshold slopes were used to determine the temperature in a device adjacent to the device being heated. Eight different geometric layouts were tested (M1S4 is the reference device). The devices and test

method are described below. The results are summarized in these tables. These wafers were supplied for the 10S model build. Wafer VF0T5TY chip 0607 and wafer VK0Q87Y chip 0705 from lot 5CB49E41AL.

Note: Two transcription errors corrected in table [redacted] Original values remain with strike-through.

PC spacing	Waf T5TY Deg C/mW/u	Waf Q878 Deg C/mW/u	Comments
Base device, PC -PC=0.26,	33.25	36.75	M1S4 - 4CA/3X
PC-PC = 0.51	18.8	19.1	M1S3 - 4CA/4X, Al bridge
PC-PC=0.98	~~3.1~~ 5.5	7.9	M1S2 - 4CA/4X, No Al bridge

Added CA	Waf T5TY Deg C/mW/u	Waf Q878 Deg C/mW/u	Comments
Base device, 4CA/3X	33.25	36.75	M1S4
6CA/3X & "cooling fins"	26.25	31.5	M2S3

Device widths / Ca/u	Waf T5TY Deg C/mW/u	Waf Q878 Deg C/mW/u	Comments
Base device, 4CA/3X, W=1.75	33.25	36.75	M1S4
2CA/3X, W=0.825	28.5	30.3	M2S1
2CA/3X, W=0.1225	3.1	0.8	M1S1

RX past device	Waf T5TY Deg C/mW/u	Waf Q878 Deg C/mW/u	Comments
Base device, RX=0.89	33.25	36.75	M1S4
RX=2.64	33.25	26.3	M3S1
RX=35.9	~~31.5~~ 30.9	N/A	M2S4

Layout of device pads

This plot shows the general layout with the pads labelled as referenced in the description of the testing. There are six pads for each structure:

Gate - Gate pad is connected to both gates

Heating force - Source connection for device which is heated

Common force - | Common drain diffusion for both devices. Force and sense refer to kelvin connection

Common sense- |

Meas force - | Source for measurement device. Force and sense refer to kelvin connection

Meas sense- |

shm1s4_mu.gif

Description of the devices measured

Description of the devices measured

Table of dimensions

Table of dimensions

Device	Ld	Wd	PC-PC	RX Length	Contacts	Comments
M1S1	0.0875	.1225	0.2625	0.8925	2/3X	Very narrow Rx
M1S2	0.0875	1.75	0.98	1.61	4/4X	wide space between gates
M1S3	0.0875	1.75	0.5075	1.1375	4/4X	medium space between gates
M1S4	0.0875	1.75	0.2625	0.8925	4/3X	Base device
M2S1	0.0875	0.875	0.2625	0.8925	2/3X	narrow Rx
M2S3	0.0875	1.75	0.2625	0.8925	6/3X	Extra contacts & cooling fins
M2S4	0.0875	1.75	0.2625	35.9351	4/3X	Very long Rx
M3S1	0.0875	1.75	0.2625	2.6425	4/3X	Medium long Rx

M1S1 GL1

M1S1 GL1

shm1s1.gif

M1S2 GL1

M1S2 GL1

shm1s2.gif

M1S3 GL1

M1S3 GL1

shm1s3.gif

M1S4 GL1

M1S4 GL1

shm1s4.gif

M2S1 GL1

M2S1 GL1

shm2s1.gif

M2S3 GL1

M2S3 GL1

shm2s3.gif shm2s3_wide_view.g

M2S4 GL1

M2S4 GL1


shm2s4.gif shm2s4_wide_view.g

M3S1 GL1

M3S1 GL1

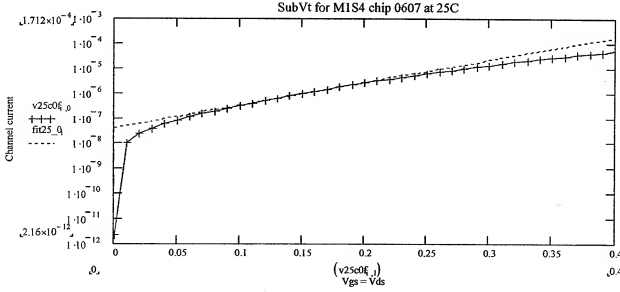
shm3s1.gif

Measurement method

Measurement method

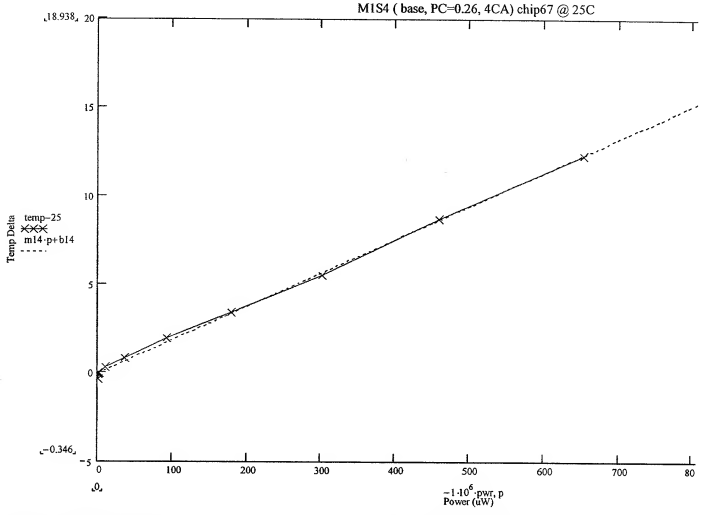
The sub Vt slope in the measurement device was used as the temperature monitor. The subvt slope versus power in the adjacent device was measured at 25C ambient. The subvt slope versus temperature was calibrated with zero power temperature measurements at 25C, 50C, 75C and 100C.

Here is a plot of data for the base device (M1S4) at 25C with no power in the force device. The devices are each tested with the gate and common diffusion at Vdd (1.0V in this case). The power device and the adjacent measurement device are forced/measured with by varying the respective sources. The common diffusion and the measurement source are connected with kelvin connections. The data for each power point is a voltage ramp of the measurement source from Vdd (1.0V) to (Vdd - 0.4V) in 10mV increments. The subVt slope is fit below Vt and above the point where the behavior becomes log-linear. For these devices Vgs = Vds = 0.1V to 0.2V was used. For reference the single point Vt is 11.25uA for this device. Here is the example:



Similar plots were constructed and the slope extracted for this device at 50C, 75C and 100C and from this the relationship between Subvt and temperature was determined.

At 25C the subvt slope for heating bias conditions of Vgs=Vds= 0 to 1V in 0.1v increments were determined. These slopes were converted to temperature deltas and plotted versus the power. Here is the plot for M1S4 on chip 0607:

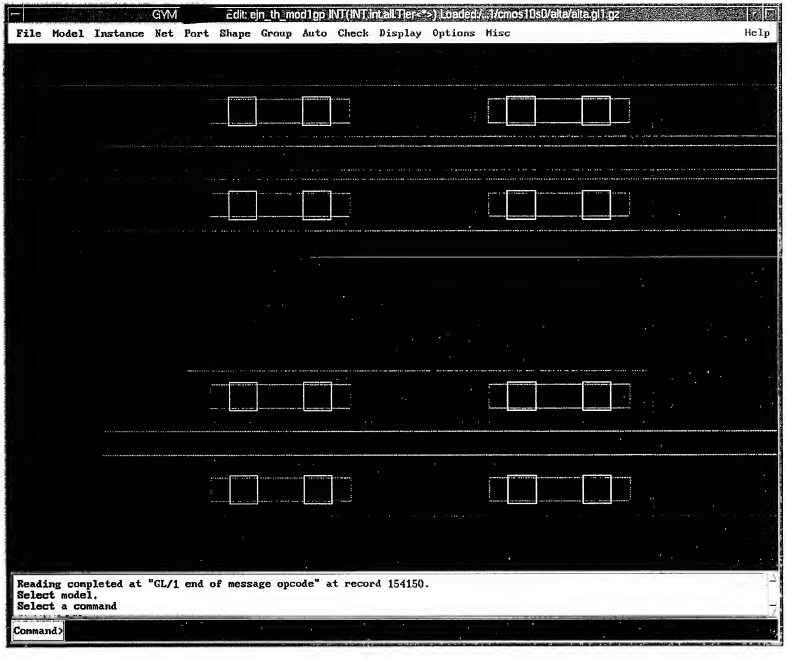


The above procedure was repeated for each device to complete the results table, which reports the slopes of these plots in degrees C/mW/u(w).

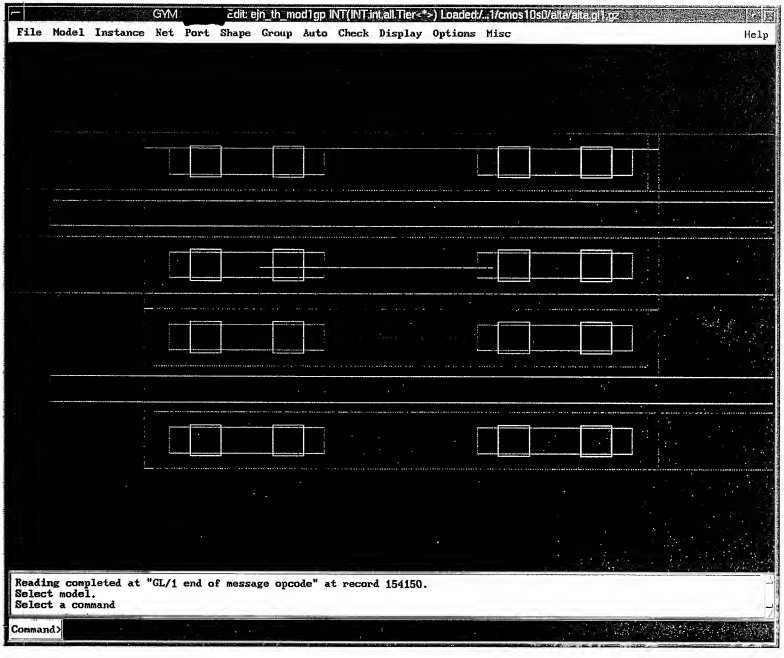
Shm1s1.gif


GVM
.dit: ejn_th_mod1gp INT(INT.Int:all.Tler<*>) Loaded:/...1/cmos10s0/alta/alta.gl1.gz
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Reading completed at "GL/1 end of message opcode" at record 154150.
Select model.
Select a command
Command>

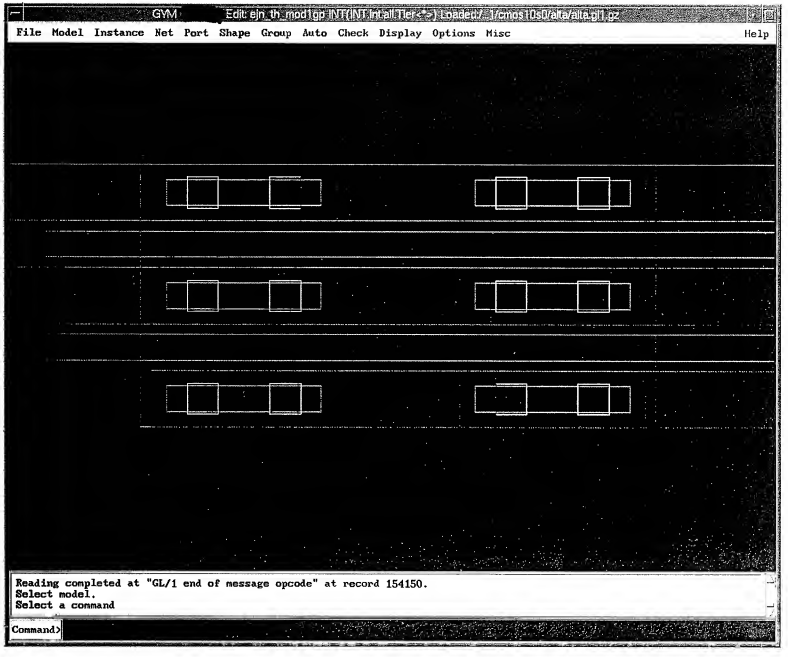
Shm1s2.gif


GVM
Edit: ejn_th_mod1gp INT(INT.inital.Ther*>) Loaded:/..7/cmos10sD/alta/alta.gl1.gz
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Reading completed at "GL/1 end of message opcode" at record 154150.
Select model.
Select a command
Command>

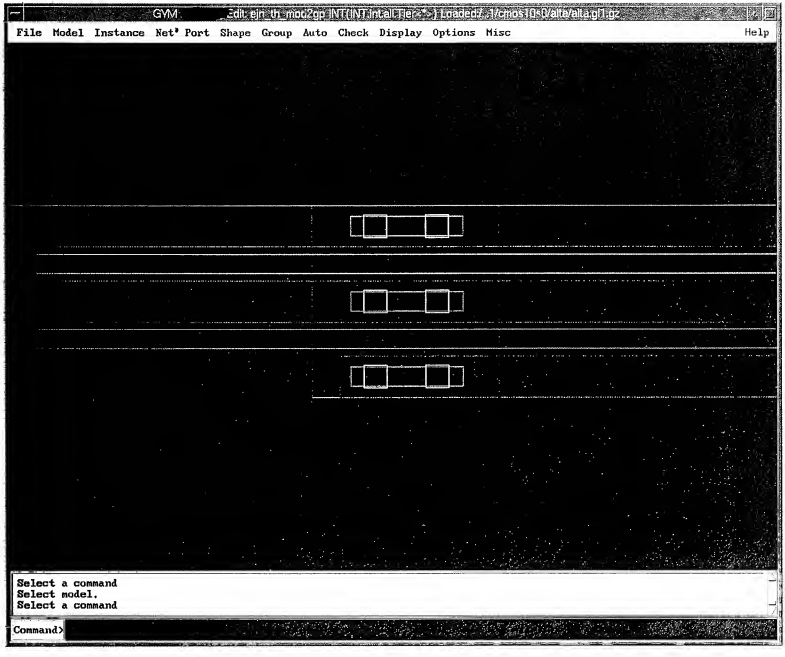
Shmls3.gif


GVM
Edit: ejh_th_mod1gp INT(INT:intall:Tier<*>) Loaded/...1/cmos10s0/alta/alta.gif.gz
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Reading completed at "GL/1 end of message opcode" at record 154150.
Select model.
Select a command
Command>

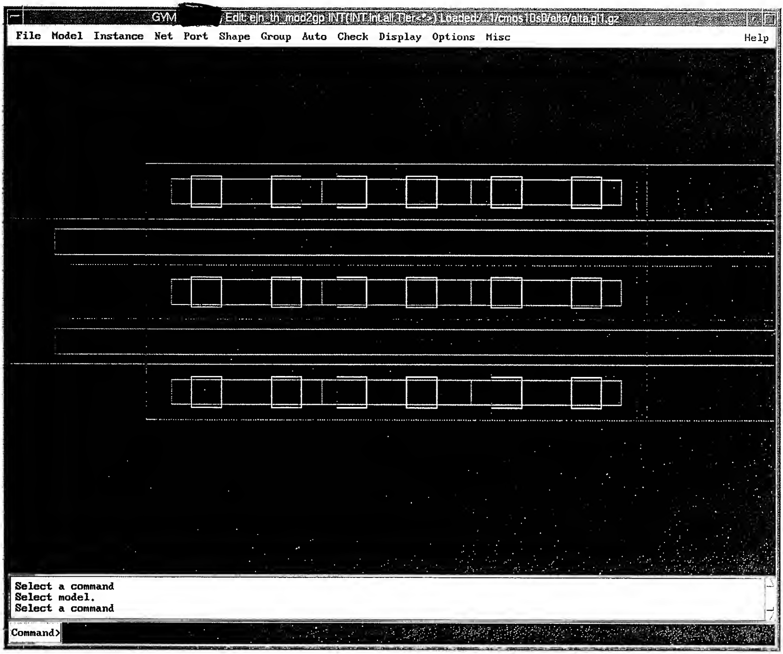
shm1s4.gif


GVM
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Reading completed at "GL/1 end of message opcode" at record 154150.
Select model.
Select a command
Command>

shm2s1.gif


GVM:
File Model Instance Net' Port Shape Group Auto Check Display Options Misc
Help
Select a command
Select model.
Select a command
Command>

shm2s3.gif


GYM [redacted] Edit: ejn_th_mod2gp INT(INT.Int.all.Tier<*>) Loaded:/..1/cmos10sD/alta/alta.gl1.gz
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Select a command
Select model.
Select a command
Command>

Shm253.gif

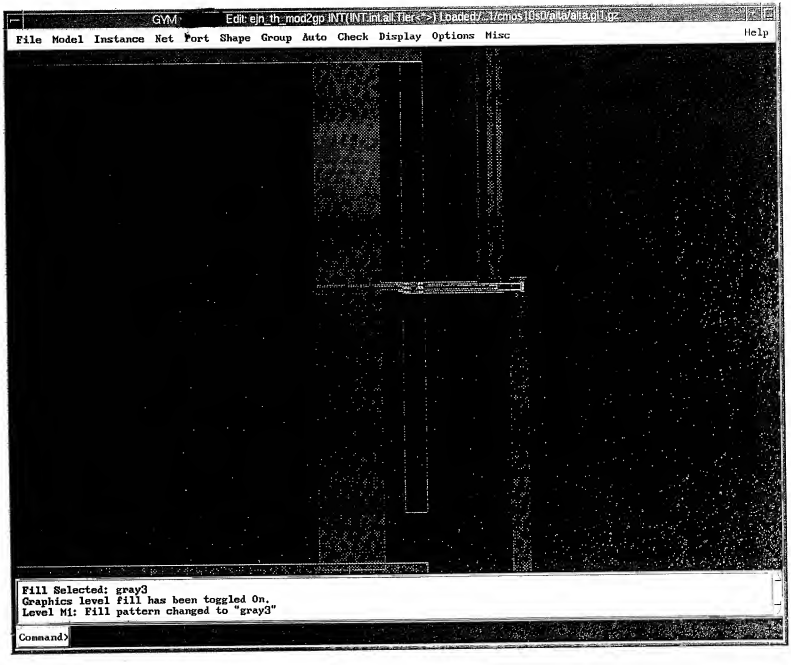
"wide view" of device

the device

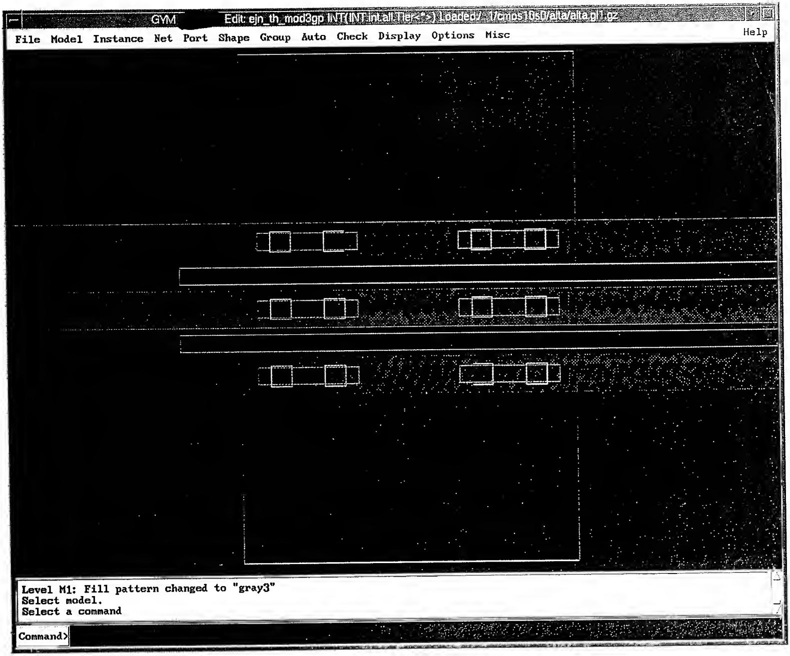
Shm2s4.gif


GVM
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Fill Selected: gray3
Graphics level fill has been toggled On.
Level M1: Fill pattern changed to "gray3"
Command>

Shm254_wide_view.gif



shm3s1.gif


GYM
File Model Instance Net Port Shape Group Auto Check Display Options Misc
Help
Level M1: Fill pattern changed to "gray3"
Select model.
Select a command
Command>